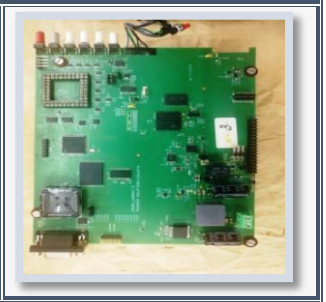
Table 1 - SATA AND U SB HARDWARE BRIDGE AND DATA PROCESSING SYSTEM



A custom hardware module that interfaces bridge between Mother Board and both mass storage devices such as SATA 2.0 HDD and USB 2.0 storage Devices that can fit in 5-1/4" bay in COTS. This included hardware, firmware, device driver software, test software,simulation software along with enclosure. It has FPGA based custom Host and Device Interfaces interconnected as a bridge between PC's mother board and HDD device, USB Device. It incorporates custom SATA-HOST, SATA -DEVICE IP cores in one FPGA for SATA interface and custom USB-HOST, USB-DEVICE IP cores in other FPGA for USB interface.

After user authentication, the system boots using an ARM Cortex A9 controller from an OTP, verifies the content of a NOR Flash holding the application code of the system and the bit stream of configuration files for SATA and USB FPGAs. Once verified, respective FPGAs are configured using SATA and USB bridges, COTS is released from power on reset to establish seamless communication with respective storage devices.

Following features:-

- **SATA Host and Device Interface for SATA Bridge**
- **USB Host and Device Interface for USB Bridge.**
- **5-1/4" Hardware Module to be fit in COTS**
- **Complete Bare Metal Programming for uC.**
- **OTP and FLASH Holding Boot Code and Application Code.**
- **Complete verification of the Boot Code and the Application code and then configuring SATA and USB bridges before booting the COTS.**
- **Flash Holding FPGA configuration Files**
- **Online FPGA reconfiguration using RS232 Interface thereby configuring the SATA and USB bridges on the next run.**
- **Online Parameter passing through separate USB2.0 uC Interface**
- **I Button security Feature through One wire interface**

- E2PROM connectivity for holding important data
- uC to OTP, FLASH, FPGA – GPMC Interface connectivity
- FLASH and SSD interf ace for FPGA Holding Storage sector information for USB and HDD
- OLED Interface
- Push Button, LEDs

ARM CORTEX A9

GPMC Interface for 16Mb OTP, 1Gb NOR Flash, Xilinx CPLD.
Point to Point 800 MHz DDR3 Interface for uC Firmware Execution.
40 MHz SPI Interface for FPGA Configuration, OLED Display.
40 MHZ SPI Interface with AT Tiny Atmega 8 bit based Sensor Network.
I²C interface for PMIC configuration.
I²C interface and One Wire Interface for I Button Authentication.
115600 bauds, RS232 Interface with COTS for remote FPGA re-configuration in NOR Flash.
I²C interface for EEPROM for board specific information.
GPIO Interface for LEDs and Switches on the front panel.
GPIO Interface for ACPI Interface for COTS.
JTAG Interface.

ARTIX 7 FPGA

SATA2.0 Device In terface with COTS using 3.125 Gbps GTPs of FPGA.
SATA2.0 Host Interface with HDD using 3.125 Gbps GTPs of FPGA.
SATA 2.0 Host Interface with 32GB SSD using 3.125 Gbps GTPs of FPGA
SPI Interface for Master Serial Configuration through ARM Cortex A9.
SPI Interface for Slave Serial Configuration through SPI Flash.
JTAG Interface.

SPARTAN 6 FPGA

USB2.0 Device Interface with COTS using external USB Device Phy.
USB2.0 Host Interface with Storage Drive using external USB Host Phy.
GPMC Controller for interfacing with 1Gb Flash.
SPI Interface for Master Serial Configuration through ARM Cortex A9.
SPI Interface for Slave Serial Configuration through SPI Flash.
JTAG Interface.